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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/596,775	06/19/2000	Se Jeong Park	00-415	4403

7590 04/07/2003
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EXAMINER

NGUYEN, HAU H

ART UNIT	PAPER NUMBER
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2676

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DATE MAILED: 04/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/596,775

Applicant(s)

PARK ET AL.

Examiner

Hau H Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02/03/2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

Response to Arguments

1. Applicant's arguments filed February 03, 2003 have been fully considered but they are not persuasive. In response to Applicant's argument about reference 6,417,860 ('860) fails to teach, disclose, suggest or render obvious the clipmap concept between a system memory and a texture cache as claimed, it is noted that this feature is not included in the claim. Instead, claim 1 only claims "fetching new texture sub-clip from an external memory." Further, there is no claimed feature about "cache memory... implemented in a hardware manner." With respect to Applicant's argument on dependent claim 4, the examiner does not rely solely on Sara reference but in combination with the texture mapping as taught in references '860 and '790. In regard to Applicant's argument that the Park fails to teach the prefetching of another texture data predicted to be used the next time in 3-dimensional space, the examiner recites from the Park reference that teach a video controller in the graphic accelerator comprising a mode register for generating a directional signal for prefetching the texture data; a prefetch controller for producing an address for another texture data predicted to be used at the next time, based on the directional signal supplied from the mode register and the address of the address generator; a memory controller for accessing the texture data corresponding to the address generated in the prefetch controller via the memory interface; and a buffer memory for storing the prefetched texture data outputted from the memory controller and the address of the prefetched texture data (col. 1, lines 57-68, and col. 2, lines 1-4). Although Park reference also teaches texture mapping in 3-D graphics (col. 1, lines 38-41), claims 5 and 6 does not claim "prediction in 3-dimensional space".

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal et al. (U.S. Patent 6,417,860) in view of Vermeulen et al. (U.S. Patent No. 5,453,790).

Referring to claim 1, Migdal et al. disclose an apparatus and method for providing texture by using selected portions of a texture MIP-map. The selected portions are referred to herein as a clip-map. Texel data relevant to a display image is stored, accessed, and updated efficiently in a clip-map in texture memory (col. 3, lines 9-14), wherein only a clip-map needs to be loaded into a more expensive but quicker texture memory (e.g., DRAM) (col. 3, lines 17-21). As shown in Fig. 3, clip-map 340 essentially consists of a set of tiles, including a pyramidal part (a first DRAM) (317-319) and a cubical part (a second DRAM) (310-316). With reference to Figs. 2 and 8A, 8B, texture MIP-map representation of a texture map is stored in mass storage device 208 (an external memory) (step 810) (col. 12, lines 24-26). Then the clip-map is selected and stored in a faster texture memory 226 (a sub-clip loader) (step 830). Using texel data stored in the clip-map, texture can be mapped quickly and efficiently to corresponding pixel data to display a new textured image (step 840) (col. 12, lines 31-37). With reference to Fig. 9, Migdal et al. also teach the texture filter 950 filters texel data sent by the texture memory according to conventional techniques. For example, bi-linear and higher order interpolations, blending, smoothing, and

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texture sharpening techniques can be applied to textures to improve the overall quality of the displayed image (col. 13, lines 55-60). Migdal et al. also teach a check can be made to prevent attempts to draw an image using texel data which is being updated. Fringe regions are defined at the edges of tiles in the cubical part of the clip-map. The fringes include at least those texels being updated. To better accommodate digital addressing, it is preferred that the fringes consist of a multiple of eight texels (col. 11, lines 36-41).

Thus, Migdal et al. teach all the limitations of claim 1, except for the DRAM having a SAM (serial access memory) ports.

However, DRAMs with SAM ports are available in prior art, one of which is disclosed in U.S. Patent No. 5,453,790 to Vermeulen et al., wherein VRAMs (dual ports memory) are built from a dynamic random access memory or DRAM and a serial access memory SAM (Fig. 5, and col. 14, lines 24-26).

Therefore, it would have been obvious to one skilled in the art to utilize the memory architecture as taught by Migdal et al. having DRAMs including SAM ports as taught by Vermeulen et al. in order to allow the display means to read the frame store memory independently from the decoding means and at its own even rate without complex addressing operations (col. 5, lines 55-59).

In regard to claims 2 and 3, Migdal et al. teach the tiles for LOD[1], LOD[2] . . . LOD[4] in the cubical part of a clip-map 440 are only updated when the eyepoint has moved two, four, eight, and sixteen pixels respectively. Because each level of detail in the pyramidal part is already fully included in the tile 415, no updating is necessary in theory (col. 11, lines 16-21).

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4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal et al. (U.S. Patent 6,417,860) in view of Vermeulen et al. (U.S. Patent No. 5,453,790) further in view of Sara (U.S. Patent No. 4,837,722).

As applied to claim 1 above, Migdal et al. and Vermeulen et al. teach all the limitations of claim 4, except for the trilinear interpolation is performed in one clock cycle.

However, Sara teaches a digital high speed 3-dimensional interpolation machine having eight RAMs required for a trilinear interpolation, wherein the necessary points for the interpolation calculation may be accessed in parallel in one clock cycle (col. 2, lines 47-52).

Therefore, it would have been obvious to one skilled in the art to utilize the interpolation machine as taught by Sara in combination with the memory system as taught by Migdal et al. and Vermeulen et al. in order to perform interpolation efficiently (col. 2, lines 32-34).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal et al. (U.S. Patent 6,417,860) in view of Vermeulen et al. (U.S. Patent No. 5,453,790) further in view of Park (U.S. Patent No. 5,990,902).

Referring to claim 5, as cited above in claim 1, Migdal et al. and Vermeulen et al. teach all the limitations of claim 5, except for the cache memory further comprises a sub-clip predictor performing a hardware-based prefetch of a sub-clip to be soon needed.

However, Park teach a video controller in the graphic accelerator comprising a mode register for generating a directional signal for prefetching the texture data; a prefetch controller for producing an address for another texture data predicted to be used at the next time, based on the directional signal supplied from the mode register and the address of the address generator; a memory controller for accessing the texture data corresponding to the address generated in the

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prefetch controller via the memory interface; and a buffer memory for storing the prefetched texture data outputted from the memory controller and the address of the prefetched texture data (col. 1, lines 57-68, and col. 2, lines 1-4).

Therefore, it would have been obvious to one skilled in the art to utilize the buffer memory as taught by Park added to the cache memory as taught by Migdal et al. and Vermeulen et al. in order to read out the texture data from the buffer memory faster (col. 2, lines 27-29).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal et al. (U.S. Patent 6,417,860) in view of Park (U.S. Patent No. 5,990,902).

In regard to claim 6, as cited above in claim 1, Migdal et al. teach a cache memory having a first DRAM and second DRAMs including a pyramidal part (a first DRAM) (317-319) and a cubical part (a second DRAM) (a clip RAM stack). Thus, Migdal et al. teach all the limitations of claim 6, except for the sub-clip prediction. However, as cited in claim 5 above, Park teaches a memory system for predicting texture data and prefetch the next texture data based on the directional signal supplied from the mode register and the address of the address generator, and a buffer memory for storing the prefetched texture data.

Therefore, it would have been obvious to one skilled in the art to utilize the buffer memory as taught by Park added to the cache memory as taught by Migdal et al. in order to read out the texture data from the buffer memory faster (col. 2, lines 27-29).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

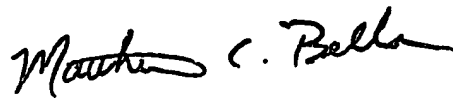
Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

04/03/2003



MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600